A Monolithic W-band Three-stage LNA Using 0.1 μm InAlAs/InGaAs/InP HEMT Technology*

H. Wang, R. Lai, T. H. Chen**, P. D. Chow, J. Velebir, K. L. Tan,
D. C. Streit, P. H. Liu and G. Ponchak***

TRW
Space and Electronic Group
M5/1085, One Space Park, Redondo Beach, CA 90278
TEL: (310) 812-8377 FAX: (310) 813-9623

ABSTRACT

A monolithic W-band three-stage LNA based on 0.1 μm pseudomorphic InAlAs/InGaAs/InP HEMTs has been developed. This LNA demonstrated a noise figure of 4.3 dB and an associated small signal gain of 19 dB at 100 GHz with a low dc power consumption of 20 mW. This is the best reported monolithic W-band LNA performance using InP-based HEMT technology and demonstrates the potential of InP HEMT technology for higher millimeter-wave applications.

INTRODUCTION

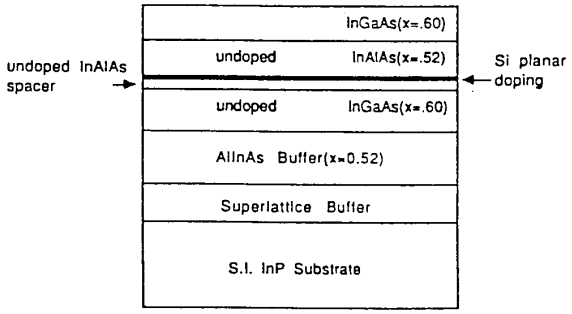
W-band low noise amplifiers (LNAs) are important components for radar and passive imaging systems applications. Development of monolithic W-band LNAs has been reported using various device technologies, including GaAs-based MESFETs [1], GaAs-based HEMTs [1]-[7], and InP-based HEMTs [8]-[10]. Among the existing device technologies, InP-based HEMTs have demonstrated the best gain and low noise performance on a discrete device level [11]-[12]. The InAlAs/InGaAs/InP material system exhibits high mobility and peak velocity and a large bandgap discontinuity between the InAlAs and InGaAs layers. These lead to higher device gain, higher cutoff frequency, lower noise figure and lower dc power consumption compared to other material systems. W-band monolithic InP HEMT amplifiers have been reported using cascode amplifier approach [8] with a gain of 8 dB and distributed amplifier approaches [9]-[10] with 5-6 dB gain around 94 GHz, but the noise figure results were not mentioned. The motivation of this work is to construct a high gain and low noise multi-stage LNA using InP-based HEMTs at W-band for low dc power receiver applications.

A monolithic three-stage W-band LNA based 0.1 μm pseudomorphic (PM) InAlAs/InGaAs/InP HEMTs is presented in this paper. This LNA demonstrated a noise figure of 4.3 dB and an associated small signal gain of 19 dB at 100 GHz with a dc power consumption of 20 mW. The gain and noise performance is comparable with the best reported results of the monolithic W-band LNA using GaAs-based PM HEMTs [5] even at this first iteration phase of the development, with a much lower dc power consumption. It consumes only 30% of the dc power typically needed in the GaAs-based HEMT LNAs with the same device periphery and design approach. This is the best reported monolithic W-band LNA using InP-based HEMT technology. With future improvements in circuit design, device modeling and MMIC processing, the performance of monolithic InP-based HEMT circuit should exceed that of GaAs-based HEMT circuits. Thus, there is excellent potential for InP-based HEMT MMICs to be inserted in W-band and higher millimeter-wave frequency band systems. In addition, this technology offers the advantage of ultra low power consumption compared with GaAs-based HEMT technology.

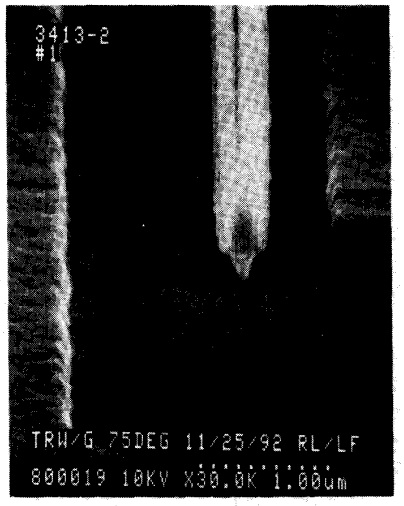
DEVICE FABRICATION AND CHARACTERISTICS

InGaAs/InAlAs/InP HEMT structure and the SEM photo of the gate are shown in Fig. 1. The high quality InP HEMT structure is grown using molecular beam epitaxy on a two-inch Fe-doped substrate. The typical room temperature and 77 K mobilities are 10500 and 35000 cm^2/V-sec respectively, with a sheet carrier concentration

*This work is supported by NASA under Contract No. NAS3-25930.
**T. H. Chen was formerly with Space and Electronic Group, TRW. He is now with Haxawave Photonic System, Inc., Hsin-Chu, Taiwan, ROC.
***G. Ponchak is with NASA Lewis Research Center, Cleveland, OH.



(a)



(b)

Fig. 1. (a) The device profile, and (b) the SEM photograph of the gate area, for the 0.1 μm PM InAlAs/InGaAs/InP HEMT device.

typically between 3.0-3.5×10^{12} cm^{-2}. Silicon planar doping is employed in the InAlAs layer to simultaneously achieve a high channel aspect ratio for a 0.1 μm gate length device and high electron transfer efficiency. Doping levels and layer thicknesses are optimized to achieve sharp pinch off characteristics, high transconductance levels and good Schottky characteristics. The device structure and layout are also carefully designed to yield minimum parasitic capacitances and resistances. All of these parameters have been found to impact the minimum noise figure of the device.

This 0.1 μm gate length pseudomorphic InP HEMTs ($In_{0.6}Ga_{0.4}As$ channel) have achieved state-of-the-art performance with a dc transconductance of 1300 mS/mm, a unit current gain cutoff frequency (f_T) of 240 GHz, an extrapolated maximum oscillation frequency (f_{max}) of 400 GHz. A measured noise figure of 1.3 dB at 95 GHz with an associated gain of 8.2 dB, and a measured gain of 7.3 dB at 140 GHz were obtained for single stage hybrid amplifiers using this HEMT devices [12]. The same device also achieved state-of-the-art performance for a Q-band hybrid cryogenically cooled amplifier which demonstrated a noise temperature of 13 K at 41 GHz [13].

The InP HEMT MMIC fabrication process was adopted from the baseline MMIC fabrication process used for GaAs-based HEMT MMICs [3]-[5], which is currently being qualified. The differences in the fabrication process steps include the device isolation process, the ohmic metallization and alloying conditions and the through substrate via hole etch. The commonality between the InP HEMT MMIC process and the GaAs-based HEMT MMIC process helps the chance of first-pass success.

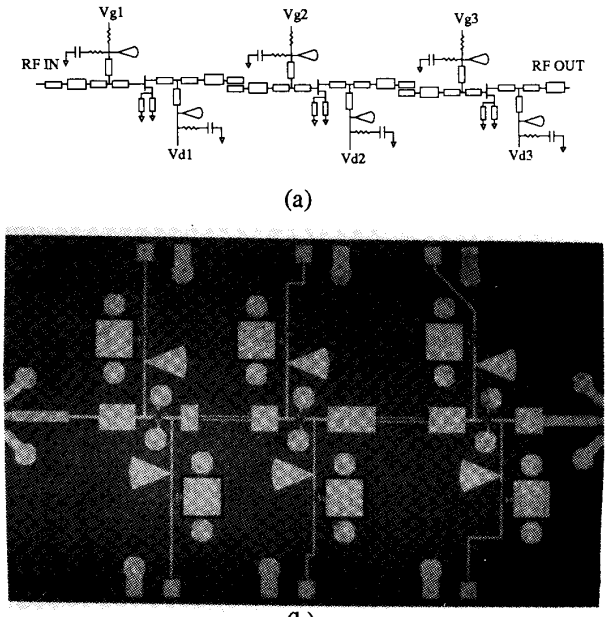
DEVICE MODELING AND CIRCUIT DESIGN

The HEMT linear small signal equivalent circuit parameters are obtained from careful fit of the measured small signal S-parameters to 40 GHz. The noise model parameters are obtained from fitting measured noise parameters to 26 GHz. These parameters are consistent with an estimation based on device physical dimensions and parameters.

Fig. 2 shows the circuit schematic diagram and the monolithic chip photograph. The size of the chip is 3.35 × 2.0 mm^2. The LNA is a three-stage single-ended design with each stage utilizing a four-finger HEMT with 40 μm total gate periphery. The input and interstage matching networks are designed for low noise figure and constructed by cascading high-low impedance microstrip lines. Edge coupled lines are used for dc blocking and radial stubs are employed for RF bypass. N^+ bulk resistors and silicon oxide metal-insulator-metal (MIM) capacitors are used in the bias networks to ensure amplifier stability. A wet chemical etching process is used to fabricate back side via holes through the InP substrated for grounding. The overall circuit design is similar to the previously published W-band monolithic LNAs [3]-[5], except that the shunt resistors on the bias networks were replaced by series RC network. This approach eliminates the dc power consumption in the bias networks.

MEASUREMENT RESULTS

The three-stage monolithic LNA were measured in a WR10 W-band (75-110 GHz) waveguide test fixture. Anti-podal finline transi-



(a)

(b)

Fig. 2. (a) The circuit schematic diagram, and (b) the photograph, of the monolithic W-band three-stage InP HEMT LNA.

tions on 125 μm thick fused silica substrate are used to couple the signal from waveguide to microstrip. The insertion loss of this transition fixture with a back-to-back transition connection is 1.5 dB. The measurement results of the LNA described below were corrected assuming the back-to-back insertion loss is equally divided between input and output of the circuit under test.

The measured small signal gain from 96 to 103 GHz and noise figure from 96 to 100 GHz for the three-stage LNA are presented in Fig. 3. At 100 GHz, the LNA demonstrates 19 dB gain and 4.3 dB noise figure. The data was taken at a drain voltage of 0.8 V and a drain current of 8 mA for each stage. The total dc power consumption of the circuit is less than 20 mW.

SUMMARY

We have demonstrated a monolithic three-stage W-band LNA based 0.1 μm PM InAlAs/InGaAs/InP HEMTs. A noise figure of 4.3 dB and an associated small signal gain of 19 dB at 100 GHz was measured with a low dc power consumption of 20 mW. This is the first reported multi-stage LNA using InP-based HEMT technology at this frequency. This first iteration has yielded comparable noise figure and gain performance of the monolithic LNA using PM AlGaAs/InGaAs/GaAs HEMTs [5] with one third dc power consumption.

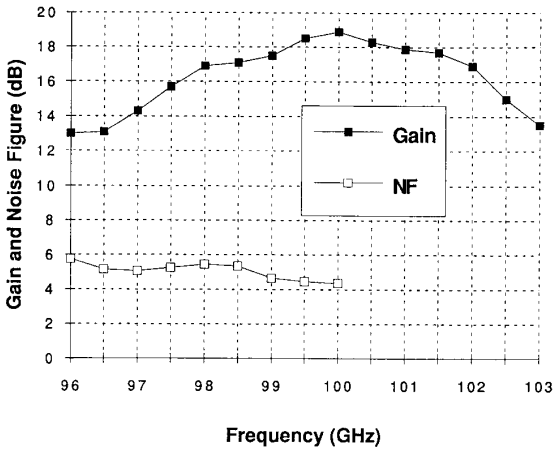


Fig. 3. Measured noise figure and associated small signal gain of the W-band three-stage MMIC LNA from 96 to 103 GHz.

ACKNOWLEDGMENT

The authors would like to thank Drs. W. Lam, J. Berenz, B. R. Allen for their discussions and suggestions, W. Bartolome for the layout effort, J. J. Raggio for the device testing, S. Bui for the assistance of via hole etching process, R. Dia for wafer processing, the MBE and EBL groups in TRW for their excellent help, and G. Hayashibara, M. Yu, D. Garske for their support of chip testing.

REFERENCES

[1] N. Camilleri, P. Chye, P. Gregory and A. Lee, "A W-band monolithic amplifier," *1990 IEEE MTT-S International Microwave Symposium Digest,* vol. 2, pp. 903-906, May, 1990.

[2] H. B. Sequeira et al., "Monolithic GaAs W-band pseudomorphic MODFET amplifiers," *1990 IEEE GaAs IC Symposium Digest,* pp. 161-164, Nov., 1990.

[3] H. Wang et al., "High performance W-band monolithic InGaAs pseudomorphic HEMT LNAs and design/analysis methodology," *IEEE Trans. on Microwave Theory and Tech.,* pp. 417-428, vol. MTT-40, no. 3, March, 1992.

[4] H. Wang et al., "State-of-the-art low noise performance of 94 GHz monolithic amplifiers using 0.1 μm InGaAs/GaAs pseudomorphic HEMT technology," *IEEE International Electronic Device Meeting Digest,* pp. 939-942, Washington D. C., Dec., 1991.

[5] H. Wang et al., "An ultra low noise monolithic three-stage amplifier using 0.1 μm InGaAs/GaAs pseudomorphic HEMT technology," *1992 IEEE MTT-S International Microwave Symposium Digest,* vol. 2, pp. 803-806, New Mexico, June, 1992.

[6] M. W. Trippe et al., "Millimeter-wave MMIC receiver components," *IEEE 1991 Microwave and Millimeter-wave Monolithic Circuits Symposium Digest,* pp. 51-54, June, 1991.

[7] H. Yoshinaga et al., "Millimeter-wave monolithic gain block amplifiers using pseudomorphic HEMT," *1992 IEEE MTT-S International Microwave Symposium Digest,* vol. 2, pp. 583-586, New Mexico, June, 1992.

[8] R. Majidi-Ahy et al. "100 GHz high-gain InP MMIC cascode amplifier," *1990 IEEE GaAs IC Symposium Digest,* pp. 173-176, Nov., 1990.

[9] R. Majidi-Ahy et al., "94 GHz InP MMIC five-section distributed amplifier," *Elect. Lett.,* vol. 26, no. 2, pp. 91-92, Jan., 1990.

[10] R. Majidi-Ahy et al., "5-100 GHz InP CPW MMIC 7-section distributed amplifier," *IEEE 1990 Microwave and Millimeter-wave Monolithic Circuits Symposium Digest,* pp. 31-34, May, 1990.

[11] K. H. G. Duh et al, "A super low-noise 0.1 μm T-gate InAlAs-InGaAs-InP HEMT," *IEEE Microwave and Guided Wave Letters,* vol. 1, no. 5., pp. 114-116, May, 1991.

[12] K. L. Tan et al., "140 GHz 0.1 μm gate-length pseudomorphic $In_{0.52}Al_{0.48}As/In_{0.60}Ga_{0.40}As/InP$ HEMT," *IEEE International Electronic Device Meeting Digest,* pp. 239-242, Washington D. C., Dec., 1991.

[13] M. W. Pospiezalski et al., "Millimeter-wave cryogenically-coolable amplifiers using AlInAs/GaInAs/InP HEMTs," to be published in *1993 IEEE MTT-S International Microwave Symposium Digest,* Atalanta, Georgia, June, 1993.